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3D Architectures

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Technology	Applications Enabled
> **Fine pitch packaging** ◆ 0.5 um W/S interposers ◆ 10 um “bumps” or ◆ FOP to support 10 um IO	> **Small high pin-count chips interconnected via an interposer** ◆ Chiplets ◆ AI ◆ Computing
> **Monolithic CMOS**	> **Improved PPA**
> **Hetergeneous monolithic**	> **Novel functionalities** ◆ E.g. Analog computing

Barriers to research

1. Cost effective technology access

- Wafer access for experiments is almost impossible
  - Possible solution? Wafer reconstitution from MPW
  - Even harder in advanced nodes
- Cost of interposers for prototyping and production
  - Now over $300k, needs to be under $100k
  - Supply chain issue
- Without technology access, we end up with overly-optimistic paper designs

2. Stability of devices made with novel materials

- e.g. Hysterisis in analog “weight” programmable resistor